What is claimed is:

1. A method of fabricating a multi-layered printed circuit board, comprising:

forming a plurality of circuit layers;

forming insulating layers before or after the circuit layers are formed; and

alternately layering the circuit layers and the insulating layers, and compressing the circuit layers and the insulating layers together.

2. The method as set forth in claim 1, wherein the forming of the circuit layers comprises:

creating via holes through a copper clad laminate;

copper-plating the copper clad laminate and walls of the via holes; and

constructing a circuit pattern on the copper clad laminate,

whereby said circuit layers are double-sided printed circuit boards.

3. The method as set forth in claim 2, further comprising plugging paste in the via holes after the copper clad laminate and the walls of the via holes are plated with copper.

4. The method as set forth in claim 1, wherein the forming of the circuit layers comprises:

creating via holes through a copper clad laminate;

copper-plating the copper clad laminate and walls of the via holes to plug copper in the via holes; and

constructing a circuit pattern on the copper clad laminate,

whereby said circuit layers are double-sided printed circuit boards.

5. The method as set forth in claim 4, wherein the via holes each have a diameter of 50 to 100 μm.

6. The method as set forth in claim 1, wherein the forming of the circuit layers comprises:

creating via holes through a copper clad laminate;

copper-plating the copper clad laminate and walls of the via holes;

plugging conductive paste in the via holes; and

constructing a circuit pattern on the copper clad laminate,

whereby said circuit layers are double-sided printed circuit boards.

7. The method as set forth in claim 1, wherein the forming of the insulating layers comprises:

creating openings through an insulating layer attached by release films;

plugging paste in the openings; and

removing the release films from the insulating layer.

8. The method as set forth in claim 7, wherein the insulating layer includes a completely hardened (c-stage) resin layer and semi-hardened (b-stage) resin layers attached to both sides of the completely hardened resin layer.

9. The method as set forth in claim 1, wherein layering the circuit layers and insulating layers is subject to a targeting and a trimming process for precisely matching the via holes of the circuit layers with the openings of the insulating layers.

10. The method as set forth in claim 9, wherein the targeting process comprising of drilling the laminate to create target holes using a x-ray beam, and the trimming process comprising of solidifying the resin and the copper foil flowing out of the laminate and trimming.

11. The method as set forth in claim 1, in which a hot press is used to compress the circuit and insulating layers to fabricate the multi-layered PCB.

12. The method as set forth in claim 1, in which a vacuum press is used to compress the laminate in a vacuum chamber using an electric heater.